

Electronics Level 2 Update

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Project Status: Cost and Schedule shows very little progress

Status of NOvA Cost & Schedule

11/23/2005

	Initial talks with Bill?	List of Tasks	Durations of Tasks	Relationships among tasks	Assign labor resources	Assign M&S \$ Resources	Add contingency	Provide L3 descriptions	Provide Task Notes
<u>WBS</u>									
Site and Buildings	X	X	Х	х	х	х		X	х
Scintillator	Х	х						X	
Fiber	X	х						X	
Extrusions	Х	х						X	
Extrusion Modules	Х							X	
Electronics	X	х						X	х
DAQ	X	х						X	х
Near Assembly	X	Х						X	
Far Assembly	Х	X	X	x	x			X	



Electronics WBS progress

	List of	Duration		Assign	Assign	Add	L3	Task
	Tasks	of Tasks	Relationships	Labor	M&S	Contingency	Descriptions	notes
2.6.1								
Specifications	X						X	
2.6.2								
APD Module	X	X	X		X		X	
2.6.3								
Readout	X						X	X
2.6.4								
Readout								
Infrastructure	X						X	X



Future

• Plan to have focused phone conferences with players in each area to refine and complete plan for production and R&D, assign tasks.



Electronics R&D

- Prototype ASIC design and layout complete (Fermilab)
 - Submitted to MOSIS for Nov28 run
 - 8 week turn-around expect end of Feb
- Readout board (Harvard)
 - Design of Evaluation board for CERN ADC underway
- APD Module (Minnesota-Harvard-IU)
 - Carrier board for APDs produced by Harvard
 - Machined at UMN
 - Mounted APDs expected ~mid-March



Electronics R&D II

- Thermal Prototyping (See Urheim talk)
- Infrastructrue (See Roger's talk)
- Documents:
 - Front-end Requirements –Completed
 - APD module requirements –Draft
 - Interface issue(joint w/ module connector)